AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at page 2 of the specification, line 20 and ending at page 3 of the specification, line 15, as follows:

In relation to the SOI structure, source/drain regions lifted up in an elevated structure are generally proposed in order to reduce the resistance of the source/drain regions. Such an elevated structure for source/drain regions is disclosed in "Transistor Elements for 30 nm Physical Gate Length and Beyond", Intel Technology Journal, Vol. 06, May 16, 2002, ISSN1535766X, pp. 42-54, for example. According to the structure disclosed in this literature, portions of source/drain regions of a silicon layer serving as an active layer in an ~~SO~~ SOI structure are lifted up so that the thickness of the source/drain regions of the silicon layer is larger than that of a channel region. Thus, the thickness of the source/drain regions can be increased while reducing that of the channel region, whereby the resistance of the source/drain regions can be reduced while improving electron mobility. According to the structure disclosed in the aforementioned literature, further, a gate electrode consisting of a polysilicon film is formed on the channel region through a gate insulator film consisting of a high dielectric constant insulator film.